REMARKS

The Applicants thank the Examiner for his helpful comments during the telephone interview with the undersigned Applicants' attorney on December 12, 2005. It is believed that the present Amendment addresses the issues raised during the interview, so as to place the application in condition for allowance. Such allowance is respectfully requested.

Claims 1-23 and 25-32 are now pending in the present application. Claims 1-16, 23, 25, and 27-29 are amended above. Claim 24 is canceled above. New claims 30-32 are added above. No new matter is added by the claim amendments or new claims.

Applicants note that the Office Action Summary continues to state that claim 25 is withdrawn from consideration. As discussed in the previous Amendment filed on August 18, 2005, Applicants believe that this is in error, in view of Applicants' Response to Species Election Requirement mailed on March 23, 2005, electing Group I, including claims 1-16, 24, and 25. Correction of the Office Action Summary is respectfully requested.

Claims 4-6 and 13 are objected to, but would be allowable if rewritten in independent form. Applicants wish to defer submission of these claims, pending consideration of the present Amendment.

The previous Amendment mailed on August 15, 2005 is objected to under 35 U.S.C. 132(a) for introducing new matter into the disclosure, for reasons stated in the Office Action at page 2. Independent claims 1, 10 and 23 are amended to clarify that a semiconductor device comprises a control signal generating circuit and an internal voltage generating circuit coupled to the control signal generating circuit. The control signal generating circuit generates a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device. The control signal is activated when the input signal indicates that the number of bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits.

Notwithstanding the amendments to the claims, Applicants respectfully submit that the

prior Amendment did not introduce new matter into the application. In the Background of the Invention section of the present specification, a conventional semiconductor device including internal voltage generating circuits for a memory cell array, a peripheral circuit, and a delay locked loop are disclosed (see Figure 1 of the present specification). The internal voltage generating circuits of the Background art compare a reference voltage VREF to an internal voltage IVC, and maintain the internal voltage IVC at the reference voltage VREF (see pages 1-2, paragraphs [0004]-[0006] of the present specification). In this manner, the conventional internal voltage generating circuit generates a constant internal voltage independently from a data input/output bit number that is received and output by the conventional semiconductor device (see pages 2-3, paragraph [0008] of the present specification). However, as the data input/output bit number increases, i.e., as a greater quantity of bits is processed, the internal voltages for the peripheral circuit and/or the delay locked loop suffer voltage drops due to a corresponding increase in the number of circuit components required to process the larger number of bits. The internal voltage applied to the memory cell array does not suffer a drop even though the data input/output bit number is increased. Slow data access speed results (see page 3, paragraphs [0008-0010] of the present specification).

The present invention, in contrast to the Background art, includes an internal voltage generating circuit that raises a level of an internal voltage (see page 14, paragraph [0050] of the present specification). Specifically, the internal voltage generating circuit receives a control signal from a control signal generating circuit, wherein the state of the control signal is changed, i.e., either a "high" level or a "low level," according to the number of bits being processed, to set the internal voltage to a reference voltage or an external voltage level, respectively (see, for example, Figure 2 and see page 9, paragraph [0030] of the present specification). In this manner, data access speed is improved in the present invention despite an increase in a data input/output bit number, since there is no level drop of the internal voltage in the internal voltage generating circuit (see page 4, paragraph [0012], and page 14, paragraph [0050] of the present specification).

These features are illustrated, for example, by the embodiments of the present invention. For example, in the embodiment illustrated at least at Figure 2, a control signal generating circuit 20 generates a control signal C having a "high" level when the number of data

bits being processed is more than a predetermined bit number and generates a control signal having a "low" level when the number of bits is less than a predetermined bit number (see Figure 2 and pages 7-8, paragraph [0027] of the present specification). When the control signal is low, the internal voltage is set to the reference voltage, and when the control signal is high, the internal voltage is set to the external voltage. Further, Figures 6-8 illustrate various embodiments of the control signal generating circuit of the present invention. For example, the control signal generating circuits of Figures 6-8 fix a state of the control signal C to a "high" level or a "low" level according to the number of data input/output bits in at least a wafer state (see page 14, paragraph [0049] of the present specification). Thus, in contrast to the Background art, which generates a constant voltage independently from a data input/output bit number, the present invention can set an internal voltage to a reference voltage level or an external power voltage according to the number of data input/output bits (see pages 14-15, paragraph [0052] of the present specification).

It is therefore believed that the specification as filed supports the amendments made by the Amendment filed on August 15, 2005. Therefore, it is believed that the Amendment did not introduce new matter into the application. Accordingly, reconsideration and removal of the objection under 35 U.S.C. 132(a) are respectfully requested.

Claims 1-29 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In view of the amendments to the claims and the foregoing remarks, it is submitted that the claims satisfy the written description requirement under 35 U.S.C. 112, first paragraph. Reconsideration of the rejection of claims 1-29 under 35 U.S.C. § 112, first paragraph is respectfully requested.

Claims 1-29 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In view of the amendments to the claims and the foregoing remarks, it is believed that the claims, as amended, satisfy the requirements under 35 U.S.C. § 112, second paragraph. Reconsideration of the rejection of claims 1-29 under 35 U.S.C. § 112, second paragraph is respectfully requested.

Claims 1-3, 7-12, 14-16, 23-24, and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishita (U.S. Patent No. 6,184,744). In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the Morishita

reference. Accordingly, reconsideration of the rejections is respectfully requested.

As described above, Applicants' invention is directed to a semiconductor device having a control signal generating circuit and an internal voltage generating circuit. The control signal generating circuit generates a control signal responsive to an input signal that is related to a number of bits being processed by the semiconductor device. The control signal is activated when the input signal indicates that the number of bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits.

It is submitted that Morishita fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed. Instead, Morishita discloses an AND circuit 1d that generates an output based on two independent signals: an activation control signal ACT and a lower detection signal SIG (see Morishita, Figure 2). There is no disclosure in Morishita of the output of the AND circuit 1d being generated responsive to an input signal related to a number of bits being processed by the semiconductor device. Instead, the activation control signal ACT of Morishita is generated with reference to the operating period of the internal circuit 3, and the lower detection signal SIG is output from the lower limit detection circuit 1a in response to a comparison between a power supply voltage ExtVcc and reference voltage Vref (see Morishita, Figures 2 and 4). Therefore, it follows that the AND circuit 1d of Morishita is not the control signal generating circuit, as claimed, since the activation control signal ACT and the lower detection signal SIG are not the input signal, as claimed, and since the AND circuit 1d does not output the control signal, as claimed.

Therefore, it is submitted that Morishita fails to teach the invention set forth in the amended claims. Reconsideration of the rejections of claims 1-3, 7-12, 14-16, 23-25, and 27-29 under 35 U.S.C. 102(b) based on Morishita is therefore respectfully requested.

In view of the amendments to the claims and the specification, and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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